ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

WIRING STRUCTURE FOR INTEGRATED CIRCUIT WITH REDUCED INTRALEVEL CAPACITANCE

Application Number :

10/709204

Confirmation Number:

3203

First Named Applicant:

Richard Wise

Attorney Docket Number:

FIS920030028us1

Art Unit:

2823

Examiner:

Julio Maldonado

Search string:

(6661094).pn

<u>Certification:</u> This Information Disclosure Statement was submitted under the following conditions, which satisfies the requirement under 37 CFR 1.97(e). The filer certified:

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

	init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
ſ		1	6661094	2003-12-09	Morrow et al.			

Signature

Examiner Name	Date		